REMARKS

Claims 10-20 were deemed allowable in a Notice of Allowability mailed December 13, 2005. Applicants have made no amendment to allowed claims 10-20. Accordingly, claims 10-20 remain pending in the application. No new matter has been added by these amendments as can be confirmed by the Examiner.

A. Allowable Subject Matter.

Applicants note with appreciation the Examiner's allowance of claims 10-20.

B. Correction of Typographical Errors.

In a Notice of Drawing Inconsistency with Specification mailed January 23, 2006, the Examiner noted certain inconsistencies between the specification and the formal drawings submitted on September 22, 2005. In particular, the Examiner noted that the specification erroneously made reference to a nonexistent Fig. 1E. Applicants appreciate the Examiner's careful examination of the present application and have made appropriate amendment to the specification.

The Examiner is encouraged to contact the undersigned at (949) 567-6700 if there is any way to expedite the prosecution of the present application.

Respectfully submitted,

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APPENDIX

Version with Markings to Show Changes Made to the Specification

Changes made to the paragraph starting on page 7, line 12:

[Figures 1A-E] Figures 1A-D are a block diagram of a four processor cluster of the type more fully described in copending application serial no. 09/373,125, and included here to illustrate the technology state from which this invention departs.

Changes made to the paragraph starting on page 7, line 16:

Figure 2 is a block diagram of the cluster of [Figures 1A-E] Figures 1A-D (shown in less detail than in [Figures 1A-E] Figures 1A-D) with multiplexed read port input and data memory in accordance with the teachings of this invention.

Changes made to the paragraph starting on page 7, line 21:

Referring now to [Figures 1A-E] Figures 1A-D, as described more completely in application serial no. 09/373,125, each cluster of four processors (Processor0, Processor1, Processor2 and Processor3) has a shared data and input memory stack to which and from which each processor in the cluster can write and read. In this exemplary emulation processor, the memory stack has 256 addressable eight- bit words. Each processor has four read ports for reading an eight-bit word from the data memory comprised of address inputs RA0; RA1; RA2; and RA3 and corresponding inputs to the four eight-to-one multiplexers whose select inputs are TAC0; TAC1; TAC2 and TAC3 respectively. One each clock cycle, the inputs of the eight-to-one multiplexer of each of the four processors receives an eight-bit word from the memory. While generally satisfactory, there are a large number of processors (e.g. 64) and a correspondingly large number of memory stacks on a single ET 4 emulator chip. Silicon real estate is in short supply and the stack memory output ports take up a lot of area on the chip.